FOVEAL MULTITARGET TRACKING AND RECOGNITION SYSTEM DEVELOPMENT

STATUS REPORT

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Prepared for:

Office of Naval Research

800 N. Quincy Street

Arlington, VA 22217-5660

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Dr. Cesar Bandera
Program Manager

Contract No.: N00014-96-C-0079

Data Item A001

Daniel G. Sentz
Quality Assurance Manager

Section 1

CURRENT STATUS OF THE SBIR PHASE II PROGRAM

DECEMBER 15, 1996—FEBRUARY 15, 1997

The development of all the components of the foveal system (sensor, multiprocessor, pointing mechanism) is progressing. Both active pixel and hybrid CCD (CCD photosensors with active pixel read-out) sensor designs are being evaluated concurrently. High sensitivity has been measured even at the small fovea receptive fields. A bad production run at Orbit caused a delay in the delivery and evaluation of test chips, so a revised sensor development schedule is now being developed and shall be presented in the next status report. The Analog Devices SHARC digital signal processor has been selected as the building block for the foveal video multiprocessor, and components have been ordered for experimental evaluation of multiprocessor configurations and digital foveal camera interfaces. The Unisight pan-tilt mechanism is ready for integration with the multiprocessor and sensor.

Progress is also being made on follow-on efforts. Amherst Systems is receiving commercial inquiries on the availability and quantity procurement of the foveal camera for industrial robotics applications. Also during the reporting period, Amherst Systems collected numerous video samples from an observation tower at China Lake (NAWC) where an outdoor version of the foveal system will be installed to monitor ground vehicles. Multiresolution detection and tracking algorithms are being evaluated at Amherst Systems using this collected video as the input data. Development of the micro-miniature spherical pointing actuator will resume next month under support from NASA Johnson Space Center (Automation, Robotics and Simulation Division).

Arrangements have been made for Dr. Cesar Bandera to attend the meeting of ONR grantees/contractors supported by the Office of Naval Research in the domain of visual computation and optical information processing.. Dr. Bandera will present on May 7, 1997 at 8:30 as outlined in the letter from ONR.

1.1 EVALUATION OF CURRENT FOVEAL SENSOR TEST CHIPS

Testing of the fourth and fifth generation test chips, whose contents were discussed in the previous status report, yielded the following additional information:

1. The new source follower charge buffer identified in the last status report was experimentally confirmed to yield a very linear response in the dynamic range of CCD signals. Furthermore, its high input impedance increases gain by reducing capacitance at the CCD output/amp input node (a smaller capacitance yields a larger voltage signal for a given charge; V=q/C).
2. The new reset signal identified in the last status report was experimentally confirmed to yield a higher dynamic range. A dynamic range of greater than six bits has been recorded from small (20×20 microns) receptive fields under low light (two lux) conditions and brief (3.5mS) integration times. This is a very encouraging result, since fast frame rates are one of the objectives of the foveal sensor demonstration (the other two being wide field-of-view and high central resolution).

3. Considerable charge leakage from the receptive field was observed. This leakage has been rectified by including a high potential guard ring around each receptive field, and shielding rexel output enable switches from light with a metal layer.
4. The analog memory/multiplexer/video signal formatter circuits work well, but must also be shielded from light, particularly the capacitors in the analog memory sample-and-hold circuit.

1.2 DEVELOPMENT OF NEXT SET OF FOVEAL SENSOR TEST CHIPS

Generation six of the sensor test chips was submitted to MOSIS on December 11, 1996. The submission consists of four chips to be fabricated using Orbit's two micron low-noise CMOS process. These chips were designed to investigate various issues raised by the test results documented in the previous status report. Because the December 11 fabrication submission date preceded the delivery of generations four and five test chips, generation six test chips do not account for the testing results documented in this status report. This has been a notorious problem with the MOSIS schedule throughout this project; the MOSIS schedule does not provide sufficient time between chip delivery and the next fabrication date to conduct tests on the chips received. Consequently, the number of complete design-fabrication-test cycles permitted by the MOSIS schedule in one year is half the total number of actual fabrication dates.

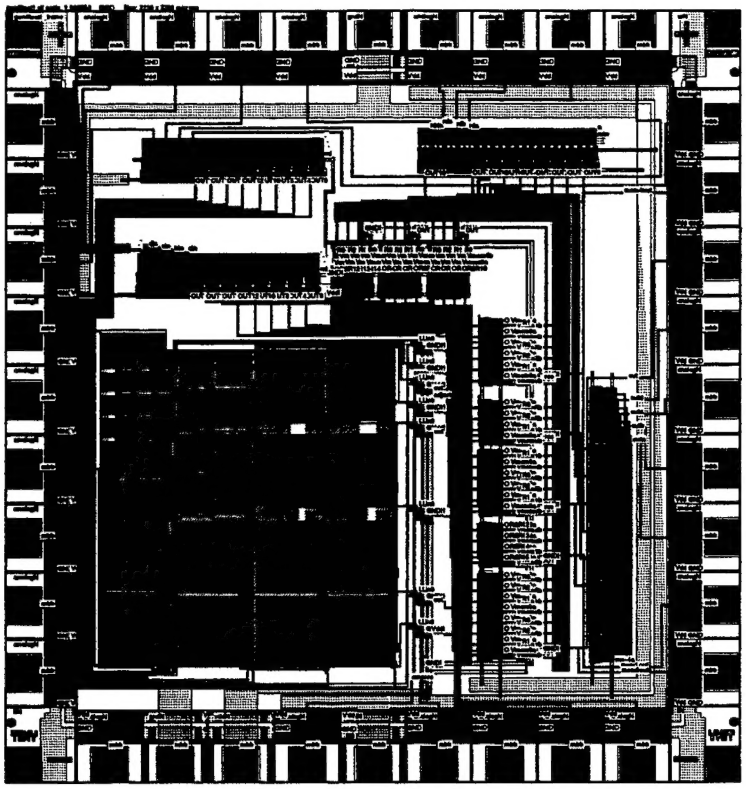
The components in the four generation six chips include CCD-amp pairs with different sensor areas, different normalizing area boundary widths and output enable areas, CCD-amp-RAAM pairs, and a complete quadrant of a foveal sensor with charge amplifier, analog memory cells, read/write control circuits and output multiplexer. Five generation seven test chips, submitted on January 29, 1997, evaluate configurations of CCD and active pixel sensor (APS) cells, and address issues 3 and 4 itemized in Section 1.1 of this report. Various combinations of light shield and guard rings are implemented in this generation. These chips are expected back by the first week of April 1997.

Generation 6 Test Chip 1:

This chip contains a full quadrant design with a fovea in the form of a 4×4 array of CCD receptive fields called drexels (Figure 1.2-1). The fovea drexels are of size 50×50 microns. Around the fovea are two discrete acuity rings with d=2, hence drexels of size 100×100 and 200×200. These larger drexels are charge normalized to 50×50. There are eight rows of CCDs. A single normalization control serves all drexels.

Read control, write control and output enable control are provided using three decoders (one for each). There are eight amplifiers in one quadrant, one for each CCD output line. The drexels falling into the same column share a common output line. There are eight RAAM banks, one for each row, and their outputs are multiplexed into a single readout line.

A common reset line drives all the CCD output lines to a independent reset voltage, which can be set at any positive value. Various test points are provided to study the signals at intermediate points in the circuit. The unity gain source follower amplifier was used in the circuit, since it has the best response for the range of CCD output voltages.



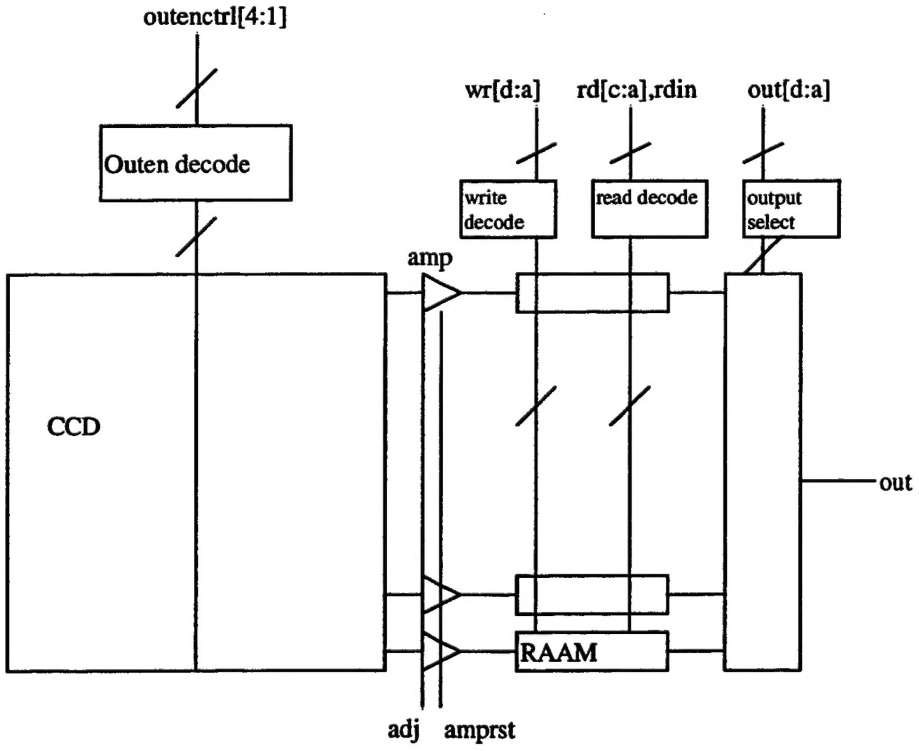


Figure 1.2-1 Layout and Block Diagram of Generation 6 Test Chip 1

Generation 6 Test Chip 2:

This chip is similar to test chip 1, but has a 4×4 array of 25×25 microns CCD elements as the fovea, and the drexels in the outer rings of size 50×50 microns and 100×100 microns respectively (Figure 1.2-2). The readout control, write control and output enable control of the quadrant is identical to test chip 1. This chip was developed to test the effectiveness of a smaller sized drexel to distinguish different light levels.

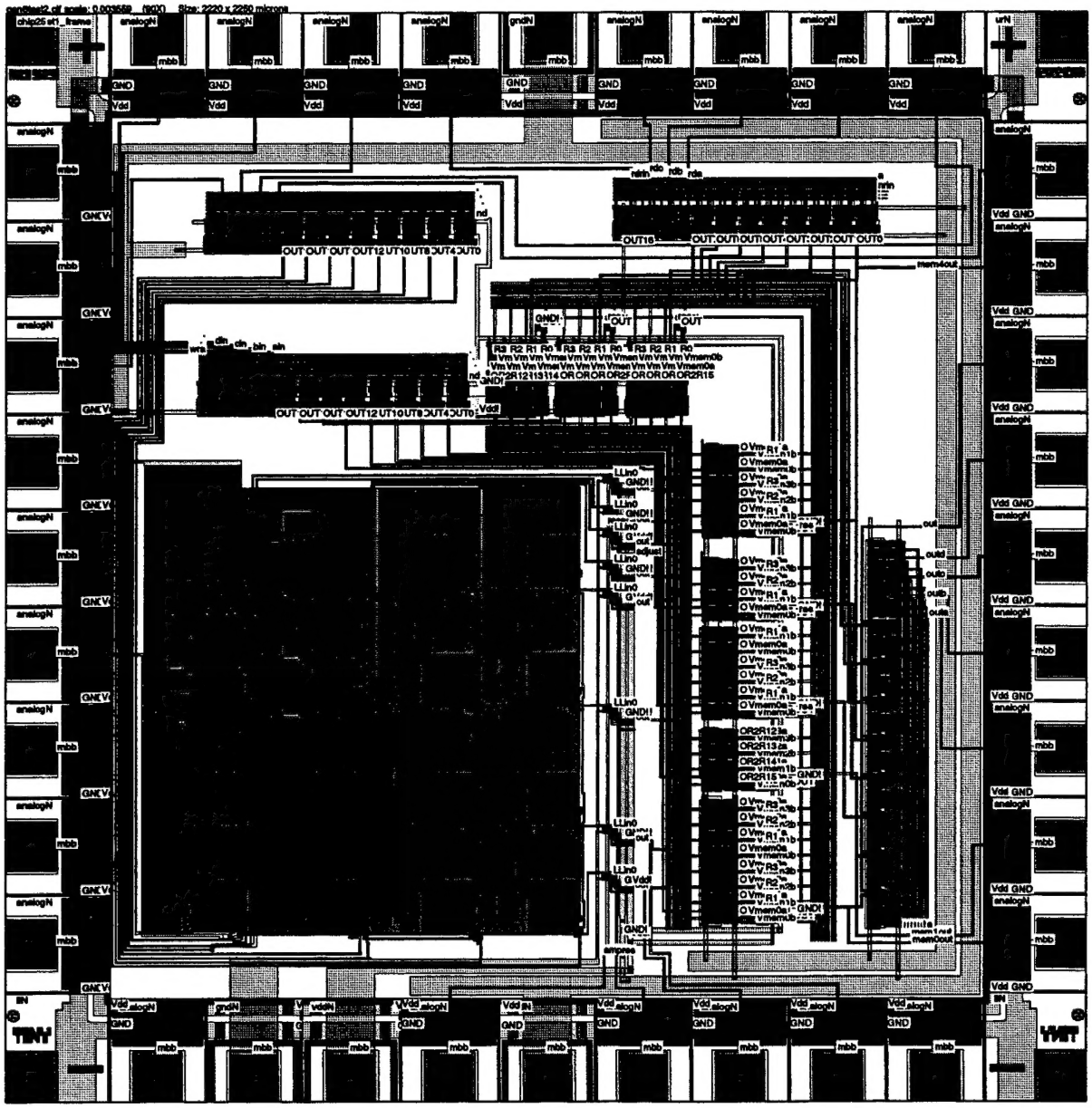
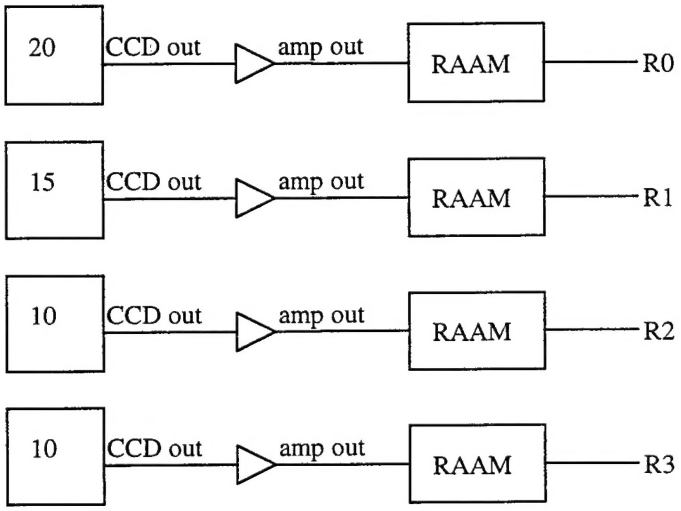


Figure 1.2-2 Layout of Generation 6 Test Chip 2

Generation 6 Test Chip 3:

This chip tests the response of 10×10, 15×15 and 20×20 microns CCD elements. It contains CCD elements of these sizes connected to source follower amplifiers, and the output of each amplifier is fed into a RAAM bank. A separate reset voltage is provided to facilitate positive reset (Figure 1.2-3). This chip will provide information as to how small we can make the fovea using commercial CMOS processes.



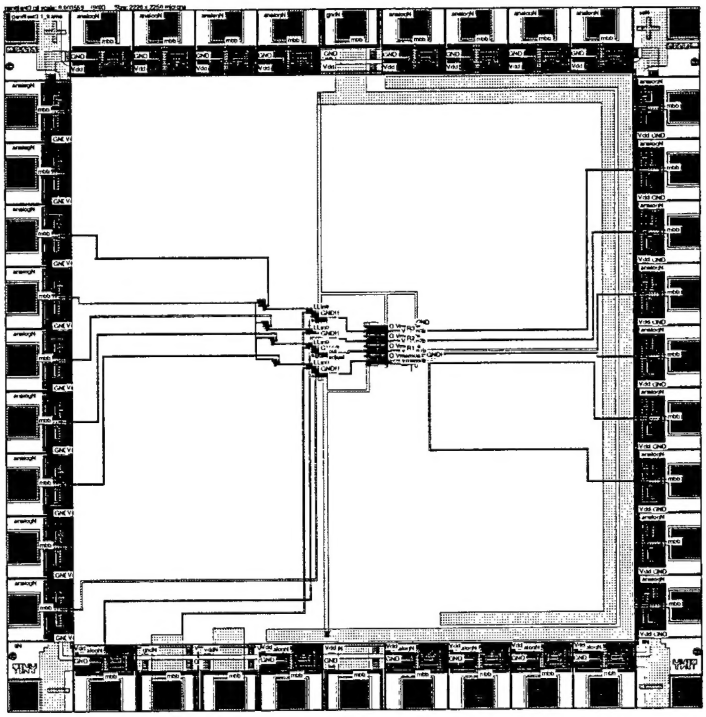


Figure 1.2-3 Layout and Block Diagram of Generation 6 Test Chip 3

Generation 6 Test Chip 4:

In this chip we change the width of the output enable pins and the width of normalizing pins to test the effect of size on their function and determine the best width for the CCD foveal sensor chip. The width of the output enable pins was changed from 2um to 4-10um and the width of the normalizing pins was changed from 2um to 5-20um. These circuits are implemented on 50×50, 20×20, and 10×10 microns receptive fields. Also in this chip, we include different source followers and a single source follower for separate testing, and different read-out lengths to evaluate their effect on signal integrity (note the bottom four drexels of the left drexel column).

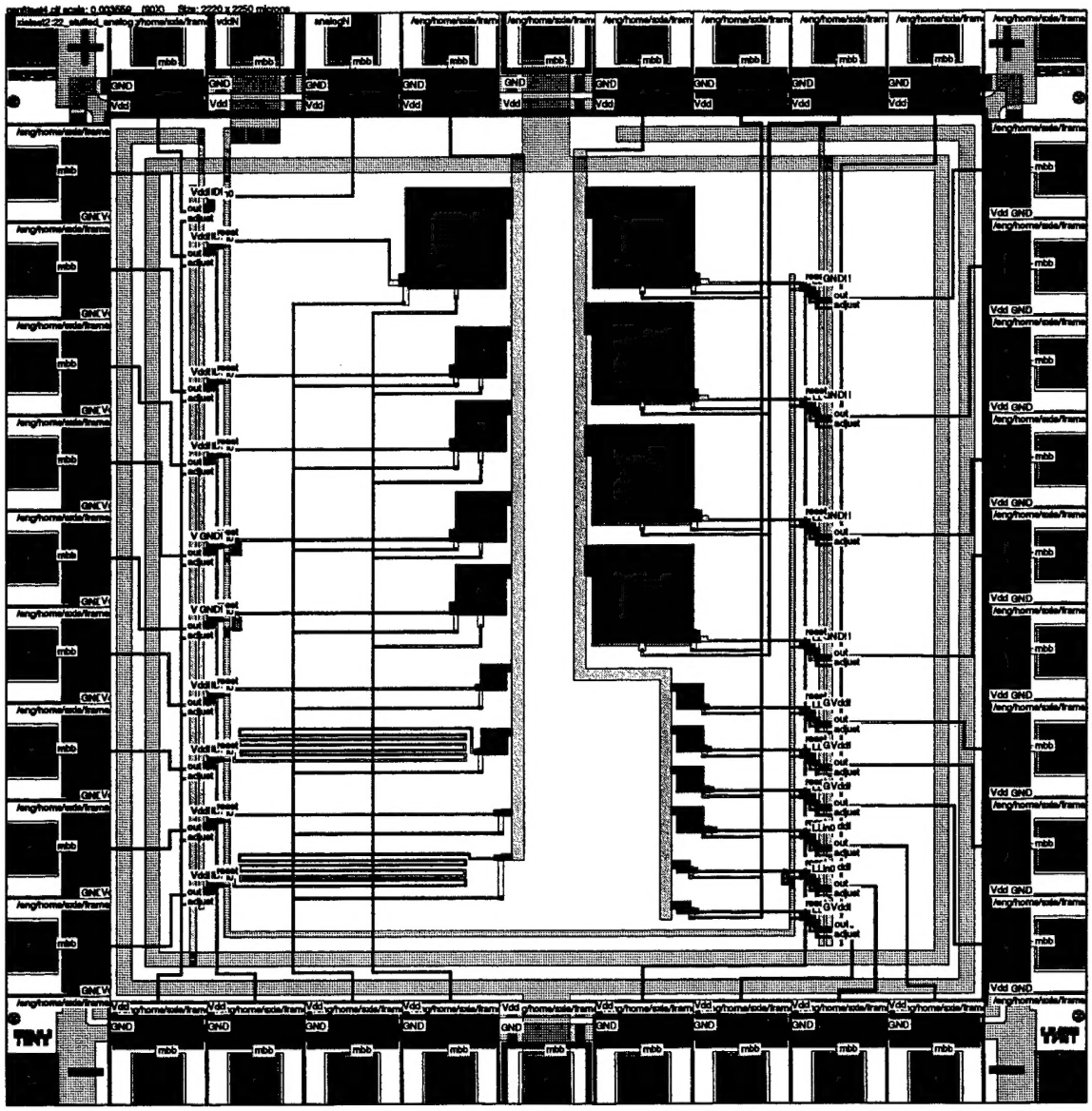


Figure 1.2-4 Layout and Block Diagram of Generation 6 Test Chip 4

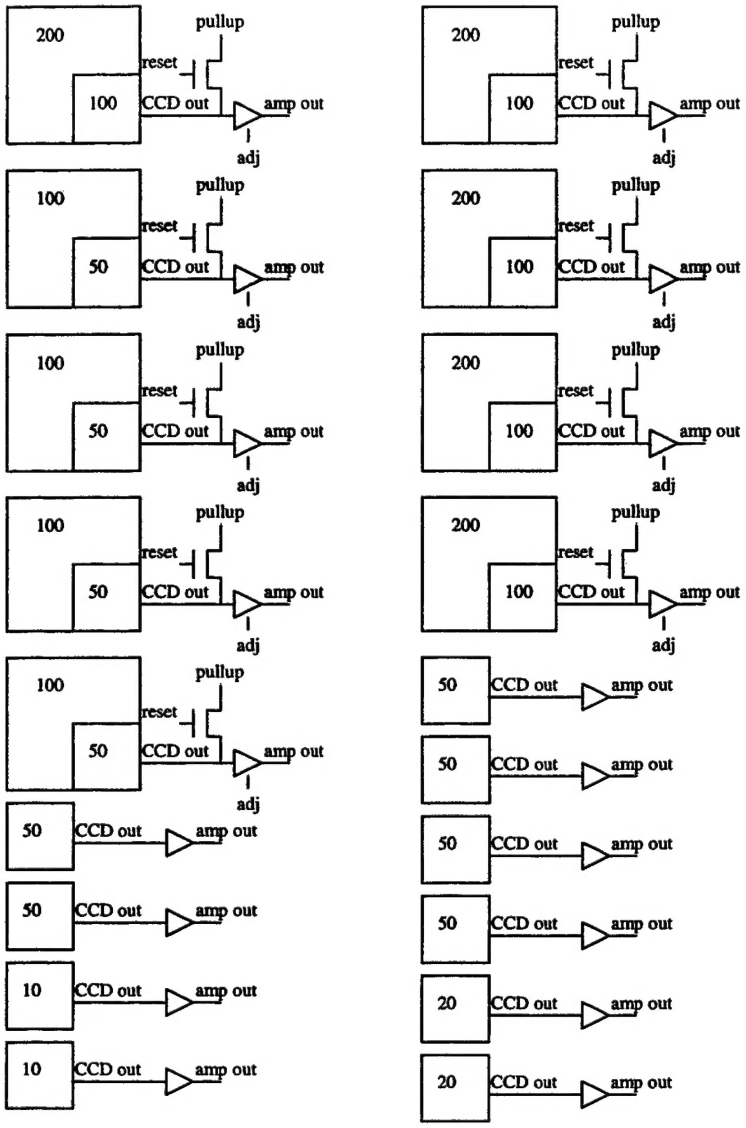


Figure 1.2-4 Layout and Block Diagram of Generation 6 Test Chip 4 (cont'd)

Generation 7 Test Chip 1:

This chip includes APS-based sensor cells of three different sizes: 20×20, 40×40 and 80×80 (Figure 1.2-5). Some of the larger two cells have normalizing gate to normalize the cells to 20×20 and 40×40. All the cells are covered with metal layers, except at the photogate area. Four modifications are added, as follow:

1. a P-diffusion guard ring,
2. floating N-diffusion in a annular fashion (larger size transfer gate),
3. wider transfer gates, and
4. wider normalizing gates.

There are five cells of 20×20, nine cells of 40×40 and six cells of 80×80. Two additional cells, one 20×20 and one 40×40, are included with metal cover on the photogate area. These two will support the experimental evaluation of the parasitic effect of light on the non-photogate areas.

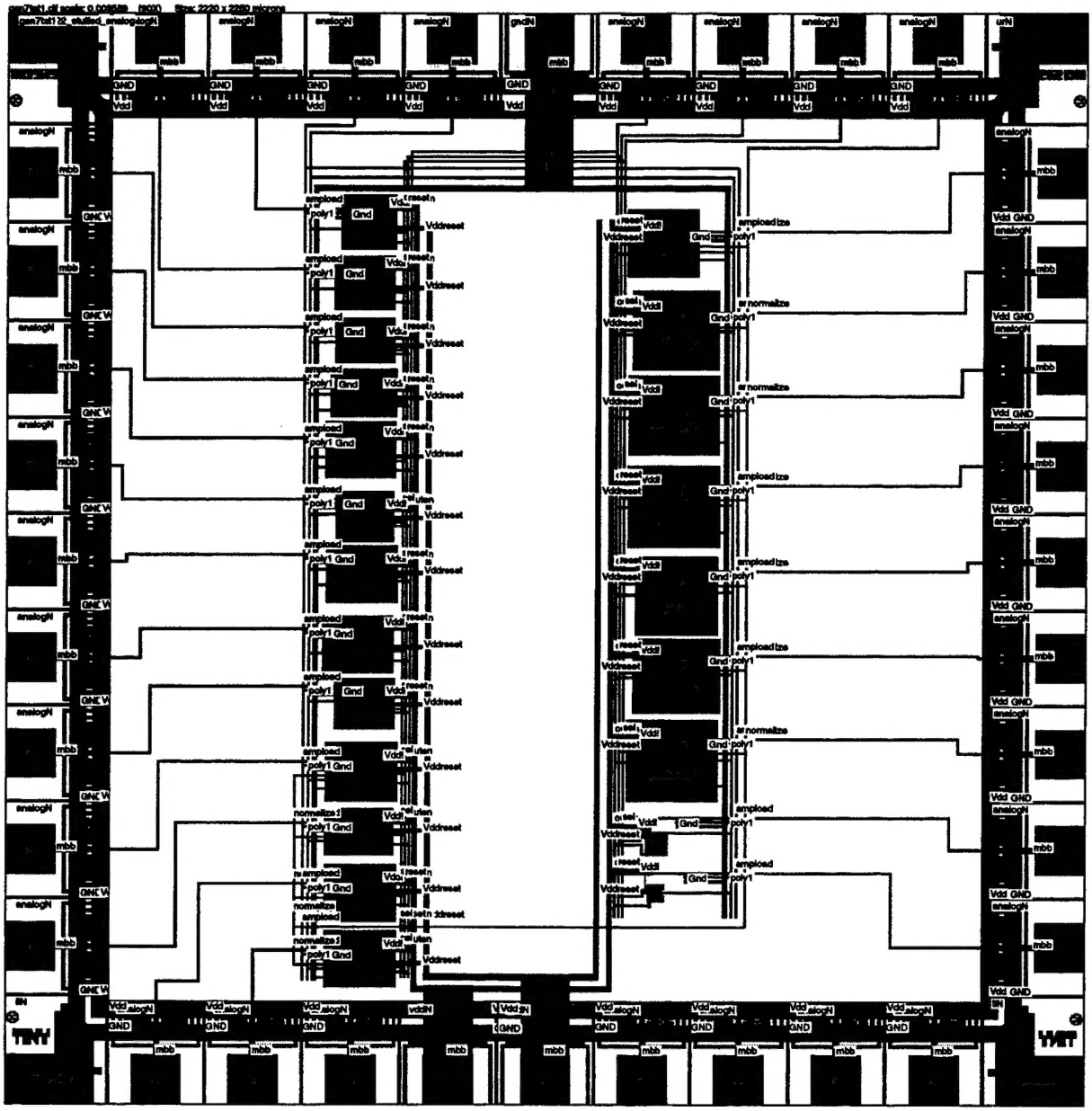


Figure 1.2-5 Layout of Generation 7 Test Chip 1

Generation 7 Test Chip 2:

This chip includes APS cells in an array fashion (Figure 1.2-6). Each row of the array has one common output, and each column has a single select line to enable the output. There area ten rows and four

columns. The lower five rows are of size 20×20. The next three rows have cells of size 40×40. The top two rows have two 20×20, one 40×40 and one 80×80 cell each. The larger two sizes have normalizing gates. Various combinations of the guard ring, N-diffusion ring, transfer gate size and normalizing gate sizes are implemented. Three different sizes of transfer gate and two different sizes of normalizing gates are implemented. All the cells except those in the lower-most row are covered by metal shield, except the photogate areas. The four 20×20 cells in the lower-most area have different areas of it covered by the metal layer to test the effect of light on different areas of the circuit.

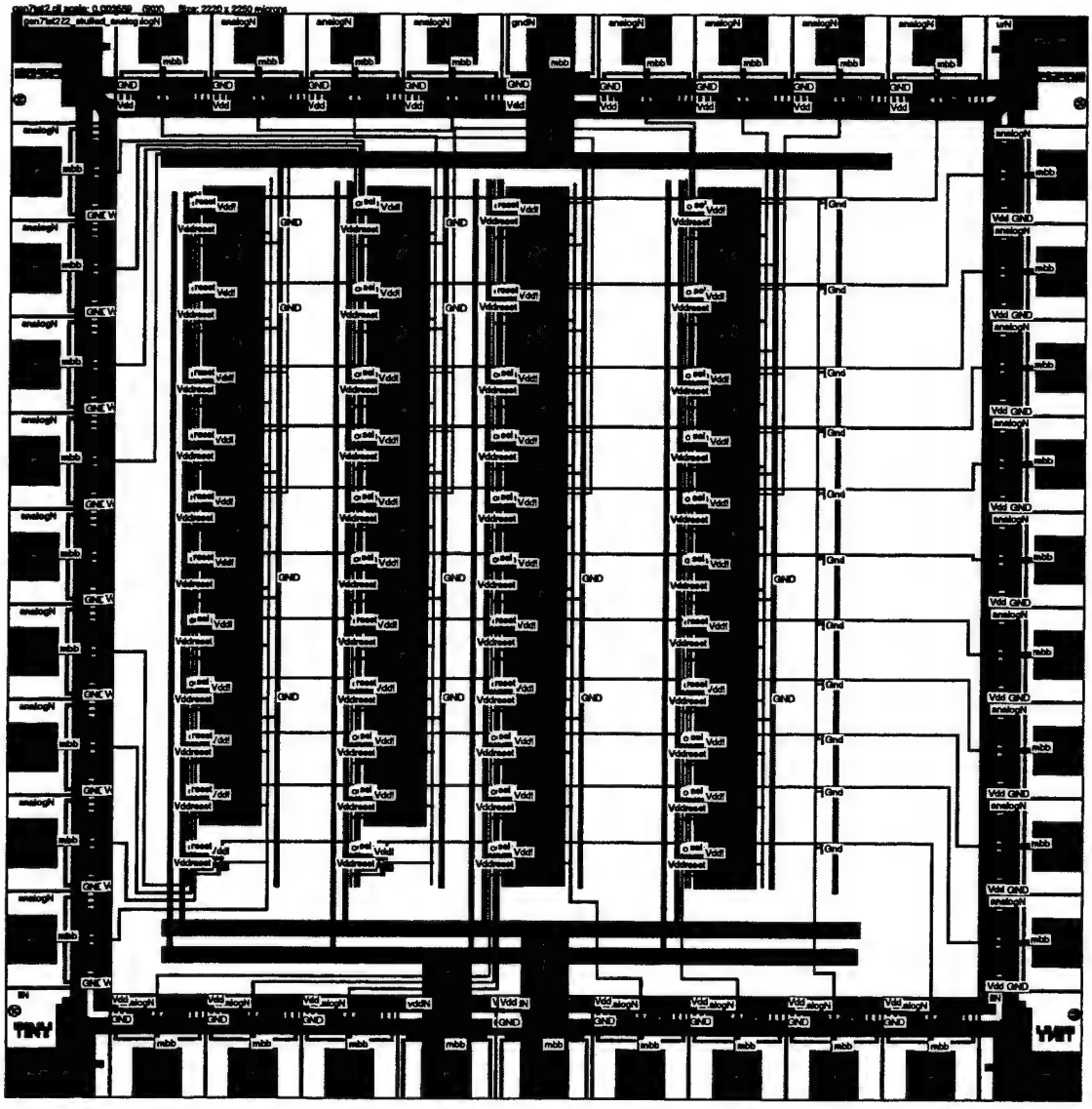


Figure 1.2-6 Layout of Generation 7 Test Chip 2

Generation 7 Test Chip 3:

During the testing of the RAAM cells in the fourth and fifth generation test chips, it was found that charge storage is affected by the incident light. This test chip implements various combinations of the RAAM cells with light shield using the metal-2 layer (Figure 1.2-7). In a previous generation chip, such a light shield was used to cover the double poly capacitors. It was found that the active diffusion areas connected to this capacitor also needs to be covered. Different configurations with common input, common output, common write, and common read are implemented. Two sections have the RAAM bank input coming from a source follower amplifier to test the configuration of a complete sensor. Also various configurations of the write enable circuit, using pass transistors as well as transmission gates, are implemented.

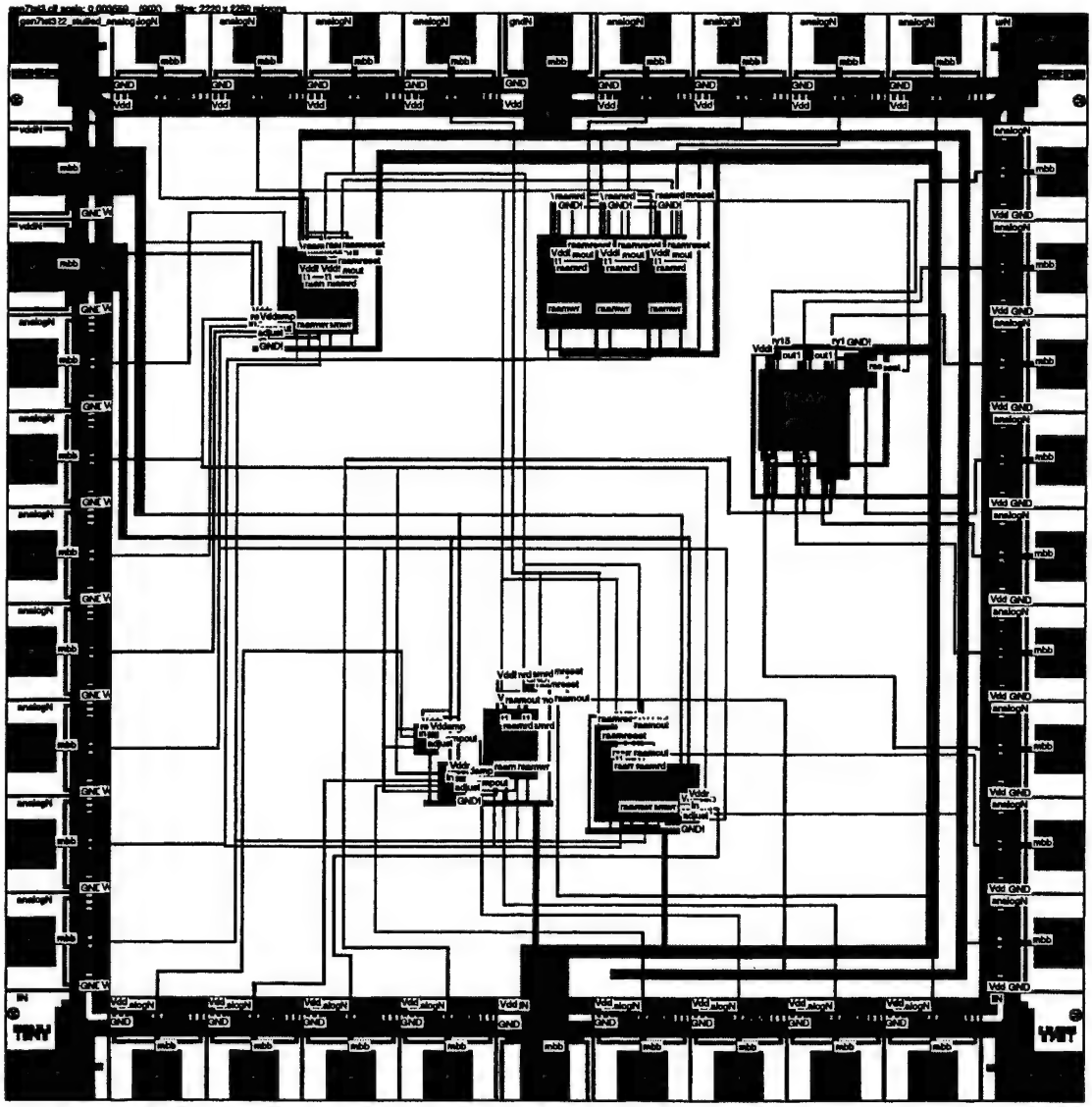


Figure 1.2-7 Layout of Generation 7 Test Chip 3

Generation 7 Test Chip 4:

This chip (Figure 1.2-8) is based on the small quadrant design submitted in December (Generation 6 test chip 1). The sensor cell array was modified by driving the charge generation poly signals column-wise. Since the cells are read out column-wise, this will allow equal integration time for every column independent of the frame rate. Also, the output enable gate widths are increased to allow for better isolation when the output enable gate is off. Similar increase is done to the normalizing gate widths. The non charge generation areas, mainly the output floating diffusion areas in the sensor section are covered with metal layer.

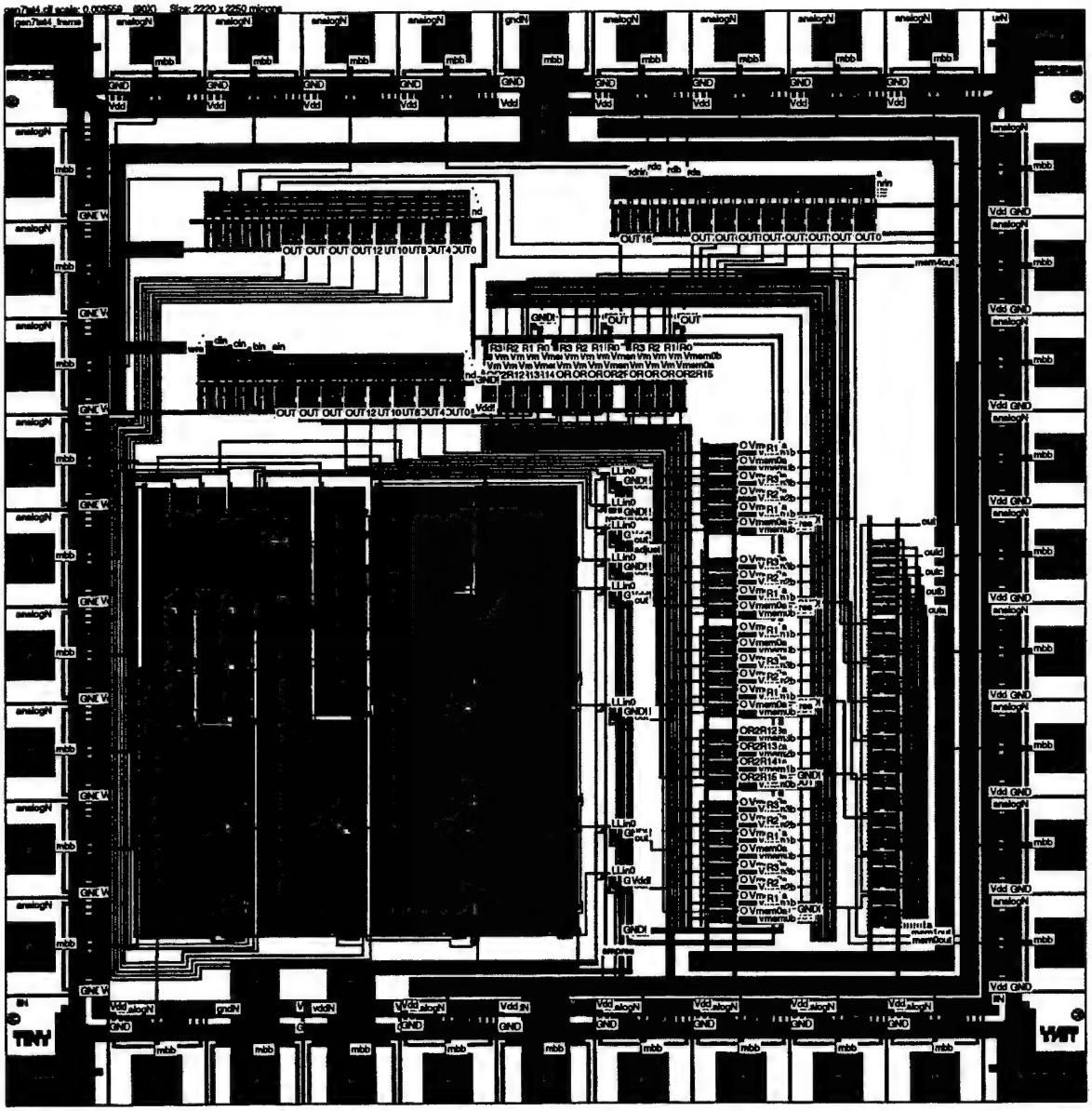


Figure 1.2-8 Layout of Generation 7 Test Chip 4

Generation 7 Test Chip 5:

Various combinations of the CCD sensors are implemented in this chip with modifications to light shield, guard ring, N-diffusion ring and larger widths of the output enable and the normalize gates (Figure 1.2-9). There are five cells of size 20×20, nine of size 50×50, and six of size 100×100. The larger cells have normalized areas of either 20×20 or 50×50. All the sensor areas except the photogate are covered by a metal layer to act as a light shield.

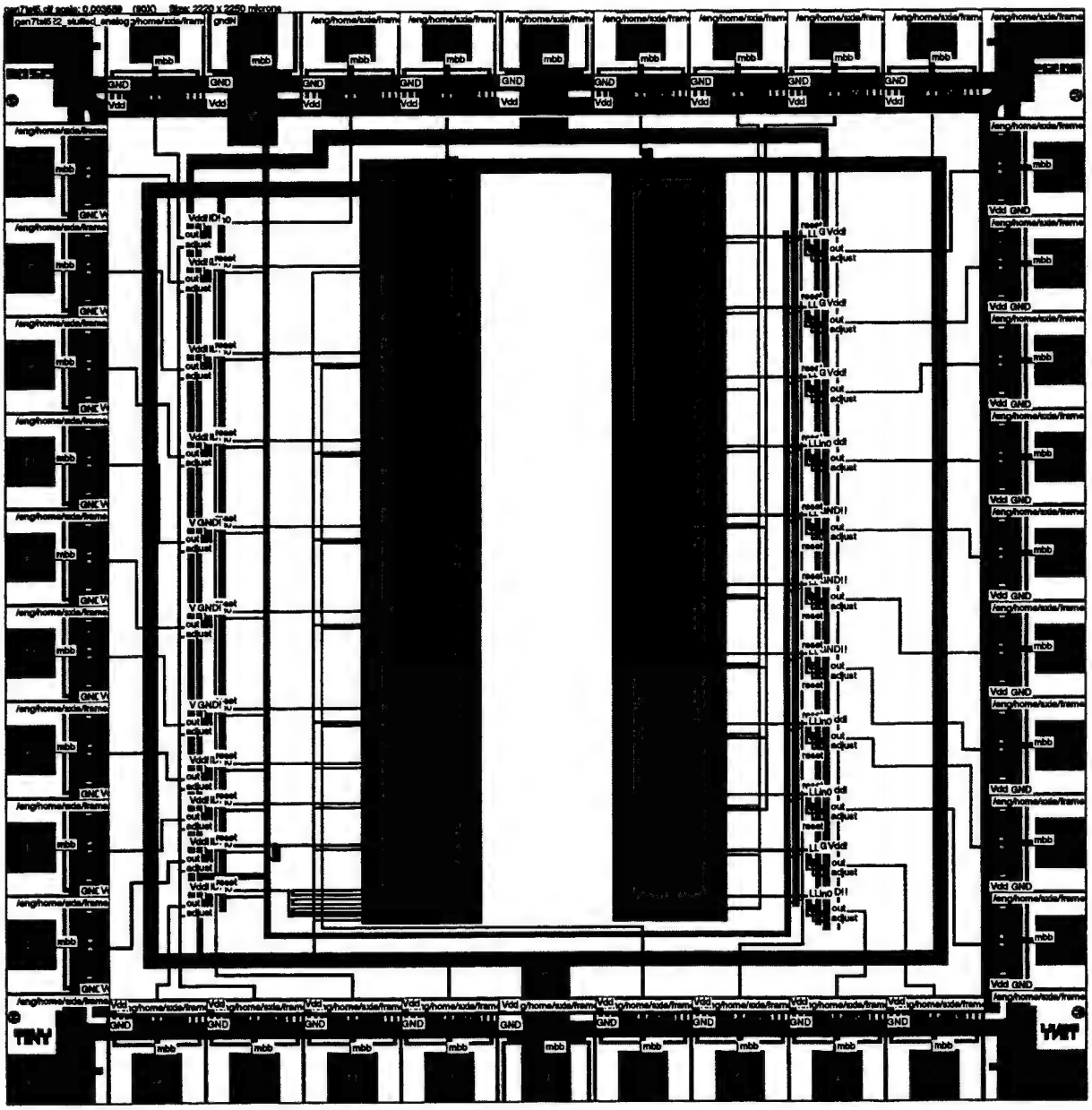


Figure 1.2-9 Layout of Generation 7 Test Chip 5

1.3 DEVELOPMENT OF FOVEAL VIDEO MULTIPROCESSOR

To perform real-time foveal vision target detection, recognition, and tracking, a multiprocessor configuration of digital signal processors (DSPs) is necessary. Our current machine vision platform consists of 24 Texas Instruments TMS320C4x class (predominantly of the 'C44 version) DSPs connected in parallel. Each 'C44 is rated at 50 MFLOPs peak, includes 64 Kbits of on-chip RAM and four 20 Mbyte/s communication ports, and accesses four Mbytes of external memory over two 100 Mbyte/s memory buses. A maximum of eight 'C44s are arranged on an ISA motherboard, giving each ISA slot 400 MFLOPs peak computing performance. Due to the rapid advances in processor architecture and performance, an Amherst Systems internal research and development project has been investigating new multiprocessor configurations to replace the 'C44 system and improve the real-time capabilities of our foveal vision and tracking algorithms.

The Analog Devices ADSP-21060 SHARC DSP is our choice for the next generation foveal multiprocessor. Each SHARC performs at 120 MFLOPs peak, contains four Mbits of on-chip dual-ported SRAM, possesses six 40 Mbyte/s communication ports, and accesses external memory over a 240 Mbyte/s dedicated bus. Alex Computer Systems in Ithaca, New York, creates multiprocessor components on the SHARC DSP that allow a maximum of 18 SHARC processors to reside on one PCI motherboard, for a peak computing performance of 2.16 GFLOPs per slot. This represents a 5-fold increase in performance per slot over the 'C44-based system. The large on-chip memory of the SHARCs allows us to store real-time foveal imagery and associated DSP code and data structures on-chip, thus freeing us from the need to buy expensive memory and eliminating the time penalty associated with external memory operations. Furthermore, Alex also supports the SHARCPAC industry standard, which specifies mechanical and electrical interface requirements industry wide and allows other vendors' daughtercards to communicate with any of Alex's products.

Software facilities for SHARC multiprocessor programming are also available. APEX is a kernel based upon the Virtuoso operating system that provides a multi-tasking environment with high level support for task-to-task and inter-processor communications. APEX is scaleable, allowing changes of hardware configuration without having to change the application source code. APEX-Lite is a smaller version of APEX that provides in-line assembly macros to ease the hardware interface. APEX-Lite offers basic functionality such as loading and downloading programs, executing code across multiple nodes, providing inter-processor communication, and creating an interface to several host environments (e.g., DOS, Windows, or UNIX). Alex also provides APEX-Lib, a library of DSP algorithms hand-coded in assembly and optimized for the SHARC processor.

An evaluation system is being ordered from Alex, including a PCI motherboard with two SHARC processors (Figure 1.3-1), a SHARCPAC module with eight processors (Figure 1.3-2), APEX-Lite utilities, the APEX-Lib DSP library, and Analog Devices' C compiler, assembler, and linker. This system will be tested on non-optimized machine vision algorithms currently running on our 'C44-based multiprocessor. The foveal multiprocessor to be ultimately used in this Phase II effort will include two PCI motherboards, two octal SHARCPACs, a digital frame-grabber SHARCPAC, a video display SHARCPAC, either APEX or the APEX-Lite utilities, the APEX-Lib DSP library, and a driver to interface the DSP multiprocessor with the Linux operating system. The complete system will include 22 SHARC processors for an estimated total cost of $55,000, or roughly $2,500 per node.

Figure 1.3-1 PCI Motherboard With Two SHARC Processors

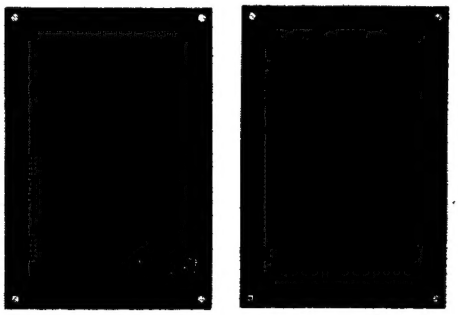


Figure 1.3-2 Bottom and Top of Octal SHARCPAC Module

SECTION 2

WORK TO BE PERFORMED FROM FEBRUARY 2 TO APRIL 2, 1997

3.1 SENSOR DEVELOPMENT AND TESTING

Additional evaluation of the in-house test chips will be performed during the next reporting period, particularly of the 1.2 micron active pixel Orbit test chips. The 1.2 micron and 2 micron active pixel chips (part of generation 5) will be compared, with the primary goals of evaluating the quality of the different VLSI fabrication processes and determining what effect fabrication and material quality can have on sensor performance. A reference test chip will also be submitted for fabrication through MOSIS under the much more expensive HP process, which is considered to be of better quality. Since only the 2 micron Orbit process supports buried CCD layers, fabrication quality tests will use active pixel circuits. The sensor development schedule will be revised to account for delays in previous MOSIS fabrications and the 1997 MOSIS fabrication schedule.

Also during the next reporting period, design efforts for the sensor support circuitry and interface logic will commence. The key aspects of this circuitry will be

1. an EPROM containing the order in which rexel values are clocked out of the sensor and the video signal format (e.g., all rexels every frame, or peripheral read-out twice as often as central read-out), and
2. digital video interface.

3.2 FOVEAL VIDEO MULTIPROCESSING DEVELOPMENT

Multiprocessor assembly and integration with the pointing mechanism controller will commence during the next reporting period. A demonstration scenario for the project will also be specified, which enhances the utility of the Phase II prototype to the China Lake target cueing installation. A Dalsa CA-D1 256×256 pixel high frame rate camera and a daughtercard with a SHARC DSP and a digital video interface (for lowpass filtering pixels into rexels) will be used to emulate the foveal camera until it becomes available. The emulator will support the field-of-view and maximum acuity of an r=2, d=2 foveal sensor, but at slower frame rates than those expected from the foveal sensor because the video stream conveys 64K pixels per frame, as opposed to 10K rexels.

SECTION 3

AREAS OF CONCERN

The sensor development schedule for 1997 is currently being revised to conform to the 1997 MOSIS chip fabrication schedule, and will be presented in the next status report. Given the limited number of fabrication runs in the MOSIS schedule, at this time we conservatively project the completion of the sensor in the fourth quarter of the calendar year. If this is confirmed during the sensor development schedule revision, then there may not be sufficient time in the current Phase II period of performance to integrate the sensor into a camera subsystem, and integrate the camera with the rest of the cueing system. Nevertheless, funds for these tasks remain secure. Consequently, a no-cost extension may be requested to accommodate the MOSIS chip fabrication schedule. Dates for final system integration and testing will be identified during the next performance period after the sensor development schedule is revised.